



IST-033709 VERTIGO

Deliverable D6.1 - Project presentation and VERTIGO web site

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ABSTRACT This document contains a short description of VERTIGO including a project synopsis according to EC formats and a set of slides presenting the project. It also includes a presentation of the VERTIGO web site

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1. Introduction

This deliverable contains a short description of VERTIGO including a project synopsis according to EC formats and a set of slides presenting the project.

This deliverable also includes a presentation of the VERTIGO web site.

2. Project synopsis

IST-033709 VERTIGO

Verification and Validation of Embedded System Design Workbench

Project URL: <http://www.vertigo-project.eu>

Coordinator	
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Project abstract

VERTIGO deals with the development of technologies and tools to integrate verification of embedded systems built upon configurable platforms, within economical and technical constraints. VERTIGO exploits results and tools coming from the IST-FP5 SYMBAD project and widens the spectrum of formal techniques applied at the verification of embedded systems.

The VERTIGO platform and its verification techniques will be assessed on a design selected by STMicroelectronics to be implemented in a System-on-a-Chip.

Objectives

The main target of VERTIGO is to reduce the verification time of embedded systems built on configurable platform, by narrowing the gap between Transactional Level (TL), that is becoming more and more popular for system level modeling, and the HDL based RT level, that represent the entry for the physical implementation.

The VERTIGO program involves several modeling, design and verification languages applied at TL and RTL, making it possible to support different methodologies for design integration onto a platform that provides a number of tools and models for IP's and communication.

A major effort in VERTIGO is to integrate dynamic and static verification around a coherent assertion based approach. Static techniques will be analysed in the context of Petri nets and High Level Decision Diagrams (HLDD) in addition to the proven SAT approach. The extension of the SYMBAD originated Property Coverage Checker (PCC) concept will be considered to serve as a framework for collecting common coverage figures.

The verification techniques developed in VERTIGO will be assessed on a design selected by STMicroelectronics to be implemented in a System-on-a-Chip.

Description of work

The project starting point is constituted by the verification core developed by the partners in the IST-FP5 SYMBAD project. This includes the AIF data-base and the Property Coverage Checker (PCC) maintained by the University of Verona, the CQuest SAT solver and the Model Checking tool maintained by University of Southampton, and the VN-Cover product based on improve-HDL provided by TransEDA.

The VERTIGO project will deliver:

- A framework of cooperation among verification techniques operating at RTL for IP verification and IP interaction targeting property & assertion verification
- A methodology to express useful properties & assertions at Transaction Level
- A framework to measure property incompleteness and an infrastructure to reliably move properties between RT and Transactional levels
- An integration of dynamic & static techniques around a coherent assertion-based approach

The main development activities will be on:

- New algorithms for SAT and SAT based hybrid solvers
- Extension of the basic Petri Nets model to include hierarchy and timing-notations
- Extension of High Level Description Diagrams (HLDD) to support behavioural level
- Adapt Extended FSM (EFSM) at capturing the behaviour of complex IP's
- Completion of the set of translators between HDL languages (VHDL or System Verilog) and AIF format
- Integration in TransEDA tool suite (imPROVE-HDL and VN-Cover) the techniques developed for RTL domain
- Assertion Coverage Checker, integrating ATPG core that can be applied at RTL and TL

Milestones and expected results

The milestones are:

- Definition of Requirements and design platform specification
- Unification of modelling and verification languages at TL1 – bus functional model
- Architecture for mixed static/dynamic verification of IPs
- Architecture for ABV applied at the system level (IP interaction) possibly at TL
- Assessment of the VERTIGO flow on a real design, including SW/HW verification at basic level

The project results will be:

- New versions of CQuest SAT solvers, new algorithms for Pseudo Boolean Optimisation (PBO) and Quantified Boolean Formulas (QBF) and new hybrid solvers. Integration of these enhancements in TransEDA tool suite

- Feasibility of application of Petri Nets and HLDDs novel techniques in the context of complex industrial verification problems. Prototypal integration in imPROVE-HDL and PCC
- The new ACC as enhancement of the existing PCC
- A verification framework based on Assertion Based Verification (ABV) providing a criterion to establish RTL vs TL equivalence based on properties
- A corresponding methodology supporting the TL / RTL validation process integrated into the VERTIGO flow
- At least 1 verified reconfigurable system selected by ST

Project details

Start date: 2006-06-01

End Date: 2008-11-30

Duration: 30 months

Project Status: execution

Total budget: 3 037 366 EUR

Total EC funding: 2 100 000 EUR

Participants	
TransEDA Technology Ltd (TransEDA Systems Ltd)	UNITED KINGDOM
AerieLogic SARL	FRANCE
University of Southampton	UNITED KINGDOM
Universita degli studi di Verona	ITALY
Linköping University	SWEDEN
Tallinna Tehnikauelkool	ESTONIA

3. Slide project presentation



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Verification and Validation of Embedded System Design

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Project objectives

- ❑ To narrow the gap between Transaction Level modeling and RT Level implementation languages, therefore reducing the verification time of embedded systems built on a configurable platform
- ❑ To integrate dynamic and static verification techniques, involving both proven SAT and novel algorithms based on Petri nets and High Level Decision Diagrams, around a coherent Assertion Based approach.
- The VERTIGO project will offer to the system designer effective means to model and verify the system according to the different options – IP models & tools – provided by the design platforms for system integration

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Starting points

- System Level design platform
- Verification core developed by the partners in IST-FP5-SYMBAD project
 - SAT technology – CQuest, MCSAT
 - ATPG and Property Coverage Checker
 - Commercial tools – VN-Cover toolsuite
 - AIF format
- Academic concepts and prototypes based on Petri nets and High Level Decision Diagrams (HLDD)

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Activities

- Develop new algorithms for SAT and SAT based hybrid solvers
- Capture complex IPs into EFSM models
- Extend Petri net and HLDD modeling capabilities
- Complete the set of translators between HDL languages and AIF format
- Develop Assertion Coverage Checker (ACC) operating at RTL and TL
- Integrate in VN-Cover toolsuite of the most effective techniques developed during the project
- Asses the VERTIGO flow on industrial design

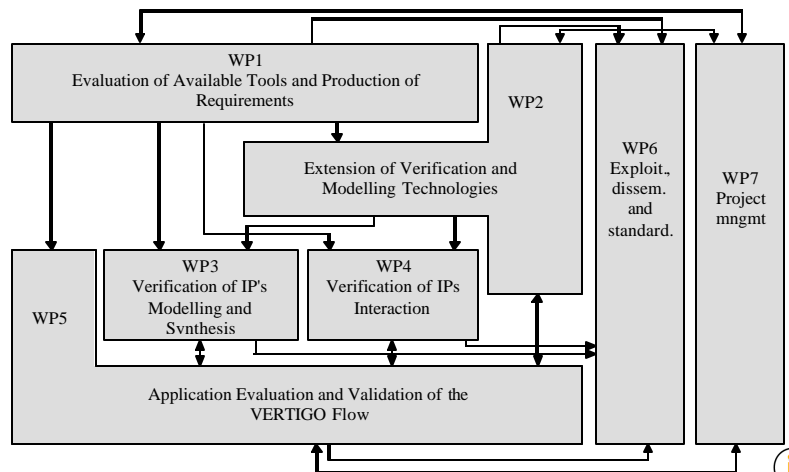
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Work organization



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The partners



STMicroelectronics Italy is the provider of the test designs & requirements and will assess VERTIGO flow on industrial test case



TransEDA is in charge of the commercial exploitation of VERTIGO results



AerieLogic is responsible of the integration of formal tools in the RTL domain



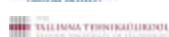
University of Southampton develops SAT based tools



University of Verona develops ATPG and ACC



Linköping University develops Petri net based modeling capabilities



Tallinn University develops HLDD based modeling capabilities

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Expected results

- New versions of SAT based solvers to be integrated in VN-Cover commercial suite
- New modeling and verification capabilities based on Petri nets and HLDD
- New ACC as a framework for Assertion Based Verification at RTL and TL
- Methodology supporting TL to RTL validation process integrated in the VERTIGO flow
- Industrial test case verified and assessment

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Expected impact

- Acceleration of the verification cycle
 - Reduction of time, costs and errors in the design flow
- leading to*
- Development of more integrated and complex while more reliable embedded systems in the fields of multimedia, communication and automotive

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4. VERTIGO web site

The VERTIGO web site has been created under the following URL: <http://www.vertigo-project.eu>.

It is divided into the following sections:

- Description of the project
- Presentation of the partners
- List of Contact People
- News Area
- Public Area
- Private Area

A set of screen shots of the VERTIGO web site are presented under below:

Home page



The Project page

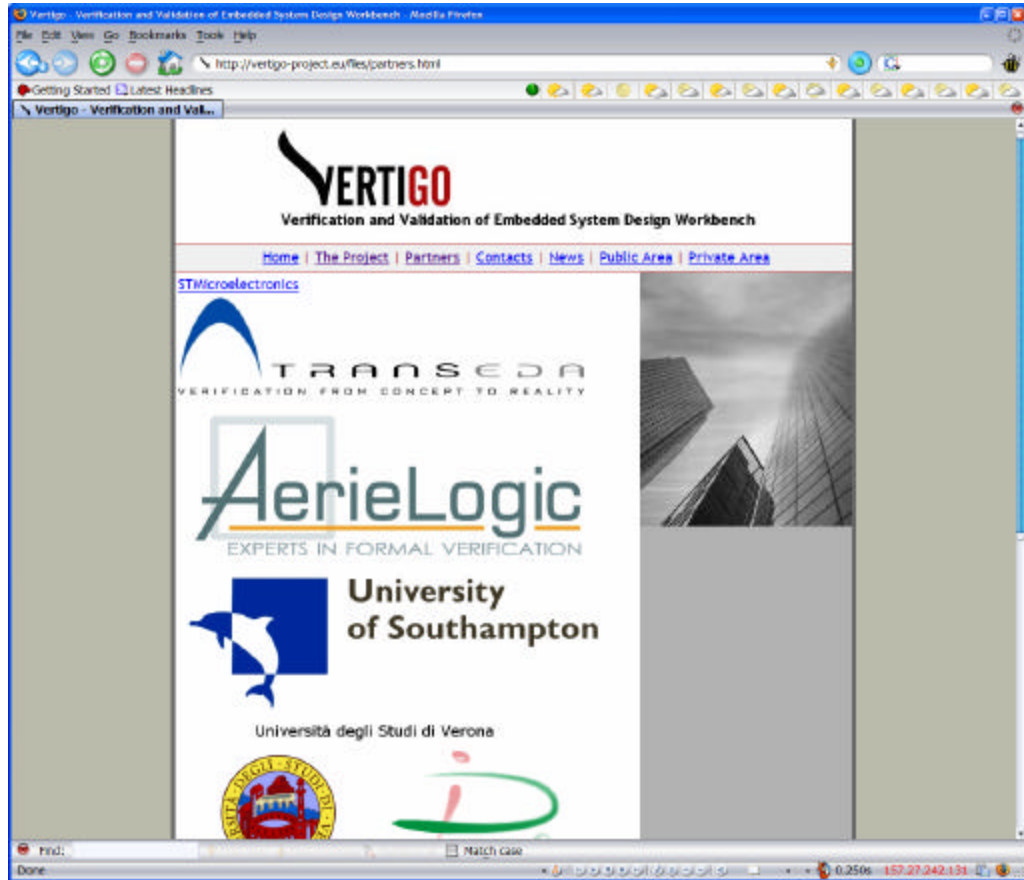
This page contains the following information:

- Abstract
- Rationale
- Vertigo Flow
- Objectives and Goals of the project
- Operational Goal and measurement of success Innovation
- Innovations of the Vertigo Projects



Partners page

This page presents the partners and their role in the project.



Contact page

This page gives the contact details of each partner of the Vertigo project.



News page

This page contains the following information:

- Events of interest for VERTIGO (events attended or to be attended by the partners)
- Publications made by the partners
- Presentations made by the partners



Public Area

This page contains publicly available stuffs (software, papers, etc.) to download



Private Area

This page automatically redirect to the eGroupware website (requires a valid account to login)

